

REMARKS

Status of the Claims

Claims 1-23 are pending.

Claims 1-23 have been rejected.

By this response, please **amend** claims 1, 5, 6, 10, 15, 16, 17, 22, 23, and **add** claims 24-29.

Rejections

The Examiner rejected claims 1-8, 22, 23 under 35USC102(b) as being anticipated by Goodman (US 2002/0073413).

The Examiner stated “Goodman teaches a parallel processor (Fig. 1, processor 105) comprising a plurality of non-volatile memory cells (113); a plurality of processor elements (115), at least one non-volatile memory cell (113) corresponding with each of the processor elements, the processor elements each accessing data from an at least one corresponding non-volatile memory cell, and performing processing on the data; and a plurality of RAM (114).

Amended claim 1 includes the following features:

a plurality of non-volatile memory cells;

a plurality of processor elements, each processor element being integrated with a non-volatile memory cell, each processor elements accessing data from a corresponding non-volatile memory cell that is most proximate to the processor element, and performing processing on the data.

(Emphasis Added)

Support for the amendments can be found throughout the specification, and more specifically, on page 4, last paragraph, where it is stated “the non-volatile memory cells 110, 112, 114, 116 can be integrated with the processor elements 120, 122, 124, 126. As will be described, the non-volatile memory cells 110, 112, 114, 116 can be magnetic memory cells. An embodiment includes each magnetic memory cell 110, 112, 114, 116 being formed adjacent to a substrate, and the corresponding processor 120, 122, 124, 126 element being formed in the substrate adjacent to the magnetic memory cell.”

Additionally, support is found on page 7, paragraphs 5 and 6, where it is stated “Figure 3 shows an MRAM cell 200 and processor element 340 according to an embodiment of the invention. The MRAM cell 200 as shown in Figure 3 is formed over a substrate 350. The substrate 350 can include a corresponding processor element 340.

As will be described, the structure shown in Figure 3 is desirable because the MRAM cell 200 does not include any transistor elements. Therefore, the MRAM cell can be formed during the conductor processing of an integrated circuit. That is, semiconductors within the substrate 350 typically include conductive lines formed over the substrate 350. The MRAM cell provides the advantage of being formed during the formation of the conductive lines. This provides ease of producing, and allows the MRAM cell 200 to be formed proximate to the corresponding processor element 340.”

Figures 3-9 also provide support for the amended claims. That is, these figures show corresponds between non-volatile memory cells and processor element that are the most proximate.

35USC102

The courts have ruled that “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. “Verdegall Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, “The identical invention must be shown in as complete detail as is contained in the ... claim.” Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Goodman provides a multi-node processing network system with a plurality of processors 105 coupled in a network 106, together with a master source 108. As illustrated in FIG. 1, the processors 105 each comprise a processor interface 112 coupling the processor in the network, a non-volatile memory 113, such as a ROM, for storing code comprising at least a boot program, a processor memory 114, such as a high speed RAM, storing a code image providing a fully operational state of the processor, and a processing unit 115 couple to the non-volatile memory 113, the processor memory 114 and the processor interface 112.

The processors 105 of Goodman are connected to the non-volatile memory 113 through an interface 112. Goodman does not teach any type of non-volatile memory cell correspondence with any particular processor. Clearly, Goodman does not teach any *non-volatile memory cell to processor element correspondence based upon the proximity of the non-volatile memory cell relative to the processor element.*

The claimed invention includes a plurality of processor elements, each processor element being integrated with a non-volatile memory cell, each processor elements accessing data from a corresponding non-volatile memory cell that is most proximate to the processor element, and performing processing on the data.

The claimed inventions allows for the benefits described in the specification in the sixth paragraph of page 7. More specifically, “the structure shown in Figure 3 is desirable because the MRAM cell 200 does not include any transistor elements. Therefore, the MRAM cell can be formed during the conductor processing of an integrated circuit. That is, semiconductors within the substrate 350 typically include conductive lines formed over the substrate 350. The MRAM cell provides the advantage of being formed during the formation of the conductive lines. This provides ease of producing, and allows the MRAM cell 200 to be formed proximate to the corresponding processor element 340.”

Goodman includes separate (not integrated) processor and memory elements. Goodman does not provide any suggestions for integration, any embodiments adaptable for integration, nor does Goodman provide any suggestion for the advantages of

integration. Goodman does not provide any discussion the advantages obtained by specifying the proximity of corresponding processor elements and memory elements.

Amended claim 1 is patentable over the cited prior art. Claims 2-21, 24-29 are directly or indirectly dependent on claim 1. Therefore, claims 2-21, 24-29 are patentable over the prior art.

Claim 5 is additionally patentable over the cited prior art because claim 5 includes the feature of the corresponding processor element is formed in the substrate proximate and adjacent to the magnetic memory cell. Goodman makes no reference of the proximity of the processor elements and the memory cells. New claim 26 includes the additional feature that the corresponding processor element is formed in the substrate most proximate to the magnetic memory cell.

Claim 6 is additionally patentable over the cited prior art because claim 6 includes the feature that the corresponding processor element and DRAM cell are formed in the substrate proximate and adjacent to the magnetic memory cell. Goodman makes no reference of the proximity of the processor elements and DRAM cells. New claim 27 includes the additional feature that the corresponding processor element and DRAM cell are formed in the substrate most proximate to the magnetic memory cell.

35USC103

The Examiner rejected claims 9-21 under 35USC103(a) as being unpatentable over Goodman in view of Young (5,621,683).

The Examiner stated” The teachings of Goodman are given in the previous paragraph of this office action. However, Goodman fails to explicitly suggest or teach an array of image sensors and an image sensor corresponding with each of the magnetic memory cells. This is what Young teaches. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of image sensor of Young into the memory substrate of Goodman because this is what Young teaches. Therefore, claim 9 would have been obvious.

Claim Rejections Under 35 USC 103(a)

It is respectfully noted that to substantiate a *prima facie* case of obviousness the initial burden rests with the Examiner who must fulfill three requirements.

More specifically:

To establish a *prima facie* case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP Sec. 2143, *In re vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Paralleling the MPEP references cited above, the Federal Circuit has enunciated several guidelines in making a 35 USC 103 obviousness determination. A *prima facie* case of obviousness is established when and only **when the teachings from the prior art itself** would appear to have **suggested** the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 783, 26 U.S.P.Q.2d 1529, 1531 (Fed Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051 (C.C.P.A. 1976)). (Emphasis added). "The mere fact that the prior art **may** be modified in the manner suggested by the Examiner does **not** make the modification obvious unless the prior art suggested the desirability of the modification." (Emphasis added) *In re Fritch*, 23 USPQ 2d 1780, 1783-84 (Fed. Cir. 1992).

Claims 9-21 are directly or indirectly dependent on claim 1. Therefore, claims 9-21 are patentable. However, claims 9-21 include additional features that make them further patentable over the cited prior art.

Young teaches a semiconductor memory element comprising a non-volatile memory transistor as a driver transistor and having an adequate difference in output signal from the cell for the different states of the memory transistor to permit the assembly of a large number of such memory cells in an array (column 2, lines 27-36). Reference is made to other thin film circuitry that may perform a logic-function and/or may comprise an active-matrix liquid-crystal display or other flat panel display and/or an image sensor.

Young does not include any suggestions of each processor elements accessing data from a corresponding non-volatile memory cell that is most proximate to the processor element, and performing processing on the data. Young makes no reference of the relative proximity of processor elements and non-volatile memory cells, or the processing of data within non-volatile memory cells. Regarding claim 9, Young makes no suggestions regarding any correspondence between an image sensor and each of the magnetic memory cells. New claim 28 additionally includes the image sensor corresponding with a magnetic memory cell is the image sensor most proximate to the magnetic memory cell. New claim 29 additionally includes the display pixel corresponding with a non-volatile memory cell is the display pixel most proximate to the non-volatile memory cell.

Claim 13 is additionally patentable over the cited prior art because claim 13 includes the features wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element formed adjacent to the non-volatile memory element. Young does not break the image sensors down to a one to one correspondence with non-volatile memory elements and processor elements. Claim 20 is patentable for similar reasons.

Claim 14 is additionally patentable over the cited prior art because claim 14 includes the features wherein each image sensor is formed adjacent to a corresponding non-volatile memory element, and each non-volatile memory element is formed adjacent to a substrate, the substrate comprising a corresponding processor element and DRAM cell formed adjacent to the non-volatile memory element. Young does not break the image sensors down to a one to one correspondence with the non-volatile memory cells, processor elements and DRAM cells. Claim 21 is patentable for similar reasons.

Independent claims 22, 23 include similar features as claim 1. Therefore, claims 22, 23 are patentable over the prior art.

No new matter has been added by these amendments.

The applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,
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